**1.**

Question 1

Fill in the blank:

The \_\_\_\_\_\_\_ Viewer is used to view designs in the simplest schematic perspective to verify logical design.

**1 / 1 point**

RTL

**Correct**

**2.**

Question 2

Power estimation post fitting using actual routing and placement information is done using which of following tools in Quartus Prime?

**1 / 1 point**



Quartus Prime Power Play Analyzer



RTL Viewer



Early Power Estimator



None of the above

**Correct**

Correct.

**3.**

Question 3

Fill in the blank:

\_\_\_\_\_\_\_ analysis can be used to find the root cause of timing violations.

**1 / 1 point**

Timing

**Correct**

**4.**

Question 4

In digital logic design, **Static Hazards** can be removed by ...

**1 / 1 point**



a. Adding additional logic to cover transitions



b. Using flip-flops and synchronous design



c. Either answer a or answer b



d. Both answer a and answer b



e. None of the above

**Correct**

Correct, either will do.

**5.**

Question 5

Which of the following statements are correct? (**Mark all that apply**)

**1 / 1 point**



Setup time is defined as the minimum time the data signal must be stable before the clock edge.

**Correct**

3 of the 4 definitions are correct.



Hold Time is defined as the minimum time the data signal must be stable before the clock edge.



Data Arrival Time is defined as the time for data to arrive at a destination register’s D input from the common clock edge.

**Correct**

3 of the 4 definitions are correct.



Clock Arrival Time is defined the time for clock to arrive at a destination register’s clock input from the common clock edge.

**Correct**

3 of the 4 definitions are correct.

**6.**

Question 6

Which of the following statements are correct? (**Mark all that apply**)

**0.75 / 1 point**



Data Required Time for setup is defined as the minimum time required before the latch edge to get latched into the destination register.



Data Required Time for hold is defined as the minimum time required before the latch edge to get latched into the destination register.



Setup Slack is defined as the margin by which the setup timing is met and calculated as Data Required Time(setup) – Data Arrival Time.

**Correct**



Hold Slack is defined as the margin by which the hold timing is met and calculated as Data Required Time(Hold) – Data Arrival Time.

You didn’t select all the correct answers

**7.**

Question 7

Which of the following can cause timing violations? (**Mark all that apply**)

**1 / 1 point**



Long data paths

**Correct**

The first 3 will cause timing violations in some instances.



Incorrect analysis of requirements

**Correct**

The first 3 will cause timing violations in some instances.



Large clock skew

**Correct**

The first 3 will cause timing violations in some instances.



Pin assignments

**8.**

Question 8

RTL Simulation is used to verify correctness of \_\_\_\_\_\_\_ ? (**Mark all that apply**)

**1 / 1 point**



Logic

**Correct**

RTL simulation is used to verify logic and sequencing.



Sequencing

**Correct**

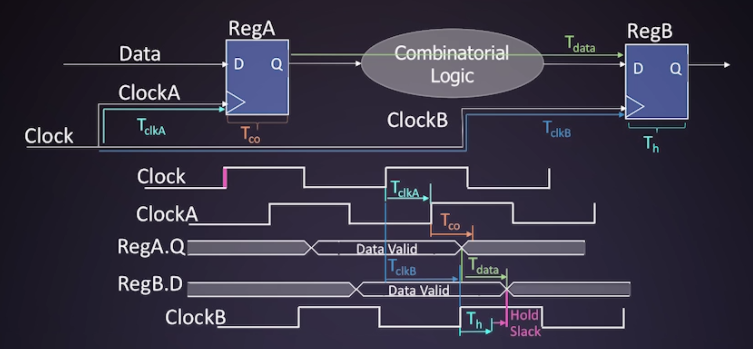
RTL simulation is used to verify logic and sequencing.



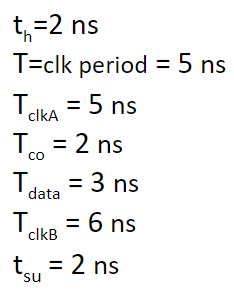
Timing

**9.**

Question 9



For the circuit above, given the following value of parameters:



What is the Hold Required Time in ns?

**0 / 1 point**



9 ns



10 ns



8 ns

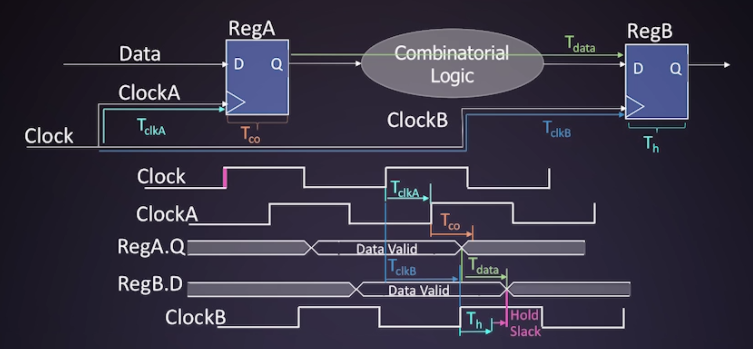


7 ns

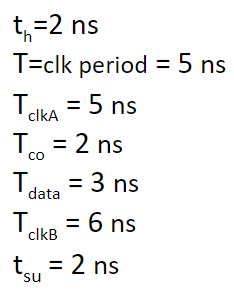
**Incorrect**

**10.**

Question 10



For the circuit above, given the following value of parameters:



What is the Hold Arrival Time in ns?

**0 / 1 point**



10 ns



5 ns



9 ns



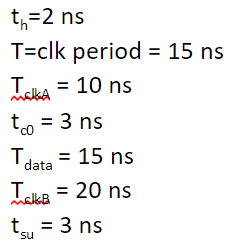
8 ns

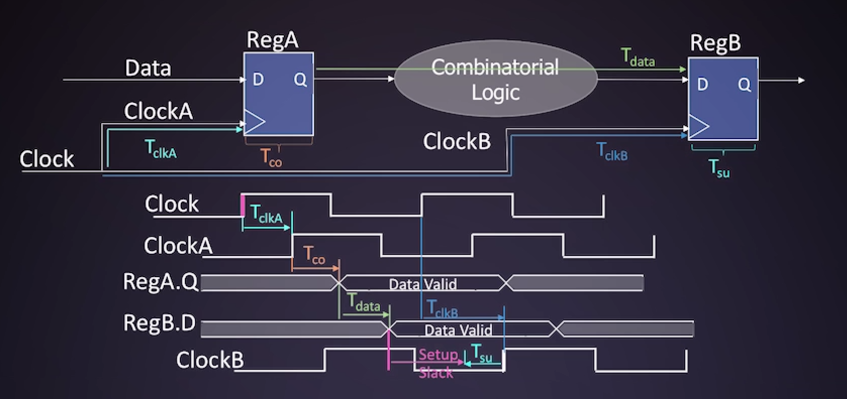
**Incorrect**

**11.**

Question 11

For the circuit in the below drawing and value of parameters:





What is the*Setup*slack time in ns?

**1 / 1 point**



-5 ns



+2 ns



+4 ns



-2 ns

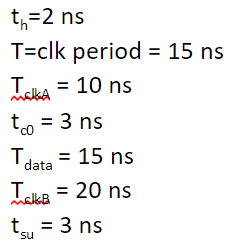
**Correct**

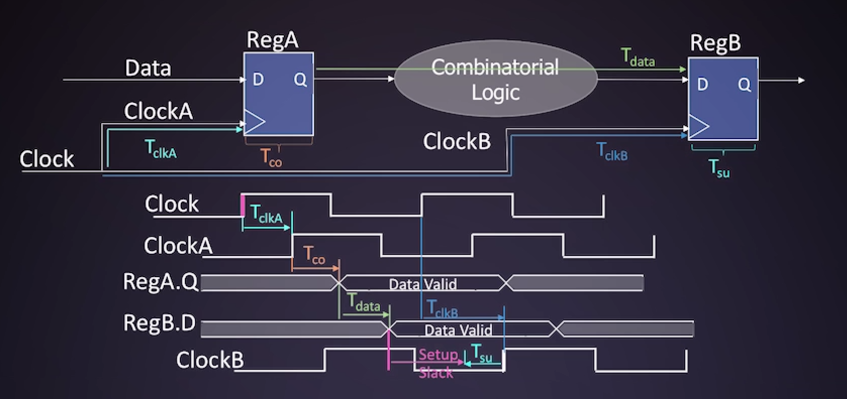
**Required Time - Arrival Time**

**12.**

Question 12

For the circuit in the below drawing and value of parameters:





Is this design safe?

**1 / 1 point**



Yes



No



Insufficient information



Either Yes or No depending on other parameters

**Correct**

When there is positive slack, the design is safe.

**13.**

Question 13

FPGA Design Flow steps include: (**Mark all that apply**)

**0.8 / 1 point**



Test and Integration

**Correct**

FPGA design steps include Test and Integration, Functional Simulation, and Programming



Deterministic Timing



Functional Simulation

**Correct**

FPGA design steps include Test and Integration, Functional Simulation, and Programming



Derivation



Programming

You didn’t select all the correct answers

**14.**

Question 14

What do you find in the Quartus Prime Task window?

**1 / 1 point**



A description of schematic tasks



Real-time task list



FPGA design flow tasks



Editor task list

**Correct**

Correct. The Quartus Prime Task window is primarily concerned with FPGA design flow steps.

**15.**

Question 15

Which one of these tools is not found in Quartus Prime?

**1 / 1 point**



Chip Planner



Signal Tap



TimeQuest



ChipScope

**Correct**

Correct, Chipscope is not a tool in Quartus, it is a Xilinx design tool.

**16.**

Question 16

Name all the methods available for FPGA logic design entry:

**1 / 1 point**



Verilog Code

**Correct**

HDL Code is a method of Design Entry



Design Entry



Schematic

**Correct**

Schematic is one way of Design Entry



.pof File



State Machine Diagrams

**Correct**

**17.**

Question 17

Static timing analysis requires a path between what number of flip-flops?

**1 / 1 point**



1



2



4



3



depends on circuit architecture

**Correct**

**18.**

Question 18

Fill in the blank:

\_\_\_\_\_\_ time is the minimum time the data signal at a flip-flop input must be stable before the clock edge.

**1 / 1 point**

Setup

**Correct**

**19.**

Question 19

In general, what is necessary to achieve optimum timing performance? (**Mark all that apply**)

**1 / 1 point**



faster flip-flops



Manual place and route



timing-driven compilation

**Correct**



well-written timing constraints

**Correct**